REMARKS

The Applicants appreciate the Examiner's care in preparing this second, non-final Office Action. To refresh the Examiner's memory as to the subject matter of the present invention, the present invention concerns a genset controller having a multiplicative gain switching device that is controlled by a processor. The processor controls the multiplicative gain switching device so that it provides a certain gain when alternator currents are at or near the rated current level, and provides a different gain when the alternator currents are significantly greater than the rated current level. Through the use of the multiplicative gain switching device and processor, a wide range of current values can be sensed accurately, especially at the lower current levels.

The Examiner set forth several grounds of objection and rejection in the Office Action. First, the Examiner objected to the drawings under 37 C.F.R. § 1.83(a) as failing to show every feature of the invention, particularly the invention as specified in pending claim 12. Second, the Examiner rejected claims 1-21 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. The Examiner's rejection in this regard particularly applied to pending claims 1, 6 and 10.

Further, the Examiner rejected claims 1, 4-5, 7-17, 19 and 21 under 35 U.S.C. § 103(a) as being unpatentable over Rice et al. (U.S. Pat. No. 6,188,203) in view of Yamaguchi (Japanese patent document no. 404000907). The Examiner additionally rejected claims 6 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Rice et al. in view of Yamaguchi and Denaci (U.S. Pat. No. 5,844,383), rejected claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Rice et al. in

view of Yamaguchi and Ashley et al. (U.S. Pat. No. 5,521,809), and rejected claims 3 and 18 under 35 U.S.C. § 103(a) as being unpatentable over Rice et al. in view of Yamaguchi and ordinary skill in the art. The Examiner further stated that, with regard to claims 4, 5, 8-9 and 11-13 "it should be emphasized that 'apparatus claims must be structurally distinguishable from the prior art'".

The Applicants will address each of these objections and rejections in turn.

OBJECTIONS TO THE DRAWINGS

In objecting to the drawings under 37 C.F.R. § 1.83(a), the Examiner particularly indicated that the "coupled between a voltage source and the additional input" of claim 12 must be shown in the drawings. The Applicants believe that the Examiner was referring to pending claim 10 rather than pending claim 12, since pending claim 10 includes the language to which the Examiner was referring. In order to improve the clarity of the language of claim 10, the Applicants have amended claim 10. In particular, the amended claim 10 makes it clear that the parallel combination of an additional feedback resistor and a combination of an additional adjustment resistor and an additional switching element is coupled between a voltage source and the additional input. This structure is clearly shown in the drawings in Fig. 5, in which the parallel combination of resistor RF2 and the series combination of resistor RA2 and switching element 516 is shown to be coupled between a voltage source 522 and a second input terminal 503. The Applicants respectfully submit that this amendment of the claim is not being made for reasons that are material to patentability, but rather is being made merely to clarify the language of the claim. Therefore, because every

element of amended claim 10 is shown in the drawings, the Applicants respectfully submit that the objection is overcome.

REJECTIONS UNDER 35 U.S.C. § 112

With respect to the Examiner's first grounds of rejection under 35 U.S.C. § 112, second paragraph, which appear to concern pending claims 1 and 6, the Applicants respectfully submit that claims 1 and 6 are definite as written. Claim 1 only recites a single "output", namely the output of the operational amplifier. Therefore, the output to which the processor is coupled must be the output of the operational amplifier. This interpretation is supported by the Specification in Fig. 5, where the processor 101 is indirectly coupled to the output 507 of the operational amplifier 502 by way of the A/D converter 248. Claim 6 is consistent with this interpretation of the output, and expressly claims the A/D converter by which the processor is coupled to the output of the operational amplifier, as supported by Fig. 5 of the Specification. Therefore, the Applicants respectfully submit that the meanings of claims 1 and 6 are definite both on their face and in view of the Specification, and so the Applicants therefore respectfully traverse these rejections of claims 1 and 6.

The Examiner additionally indicated that claim 10 was indefinite. In view of the amendment to claim 10, which was explained in more detail above, the Applicants respectfully submit that claim 10 is now sufficiently clear and definite to overcome the Examiner's rejection.

REJECTIONS UNDER 35 U.S.C. § 103(a)

In the 5th paragraph of the Office Action, the Examiner rejected claims 1, 4-5, 7-17, 19 and 21 under 35 U.S.C. §

103(a) as being unpatentable over Rice et al. in view of Yamaguchi. The Applicants respectfully traverse the Examiner's rejection, for several reasons. First, each of pending independent claims 1 and 14 recites a processor that controls the operation of a switching element in association with an operational or differential amplifier. Similarly, pending independent claim 11 recites a processing means that controls a modification means that adjusts the operation of an amplification means.

In contrast, the Applicants are unable to find any disclosure, within either Rice et al. or Yamaguchi, of a processor controlling a switching element in association with an amplifier. Although Yamaguchi appears to disclose a switching element coupled between input and output terminals of an operational amplifier, the Applicants are unable to find any disclosure of a processor controlling the operation of that switching element. As for Rice et al., the Examiner recognized and stated that this patent does not disclose a switching element in parallel with a resistor that are coupled between input and output ports of an operational amplifier. That is, Rice et al. apparently fails to disclose usage of an operational amplifier involving a variable gain. Because Rice et al. apparently fails to disclose an operational amplifier with a switching element between its input and output ports, Rice et al. further fails to disclose a processor that controls operation of such a switching element.

Second, each of pending independent claims 1 and 14 recites that the processor controls the operation of the switching element associated with the amplifier based upon an indication of an alternator current level. Additionally, the Applicants have amended claim 11 so that it similarly recites that a processing means that controls a modification means for

adjusting the level of amplification by an amplification means based upon an indication of alternator current level.

In contrast to these limitations of pending claims 1, 11 and 14, neither Rice et al. nor Yamaguchi appears to disclose a processor that controls the operation of a switching element based upon an indication of a current level from an alternator. Rice et al. apparently fails to disclose an operational amplifier with a switching element between its input and output ports. Consequently, Rice et al. further fails to disclose a processor that controls operation of such a switching element based upon a current level from an alternator. The Applicants also are unable to find any disclosure within Yamaguchi teaching that the switching of the switching element should be controlled based upon a current level from an alternator. Indeed, the Applicants are unable to determine within Yamaguchi any particular basis for controlling the switching element.

Therefore, for at least these reasons, the Applicants respectfully submit that Rice et al. and Yamaguchi, both alone and in combination, fail to disclose all of the limitations of pending claims 1, 11 and 14. As stated in the MPEP Section 2143.03, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art" (citing *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494,496 (CCPA 1970)). Consequently, because Rice et al. and Yamaguchi fail to disclose all of the limitations of pending claims 1, 11 and 14, the Applicants respectfully submit that these claims are allowable under 35 U.S.C. § 103(a).

However, even if it is found that Rice et al. and Yamaguchi do disclose all of the limitations of pending claims 1, 11 and 14, the Applicants nevertheless respectfully traverse the Examiner's rejection of these claims under 35 U.S.C. § 103(a). In order for claims 1, 11 and 14 to be found

obvious in view of Rice et al. and Yamaguchi, there must be a suggestion to combine the references to arrive at the Applicants' claimed invention. See MPEP Section 2143, first paragraph. The Applicants respectfully submit that there is no such suggestion to combine Rice et al. and Yamaguchi to arrive at the Applicants' invention as recited by claims 1, 11 and 14. Indeed, the Applicants submit that the teachings and purposes of Rice et al. and Yamaguchi are completely unrelated to one another and unrelated to the Applicants' claimed invention.

Each of Rice et al. and Yamaguchi fails to provide a suggestion to combine one another because each of these references addresses an entirely different problem. The operational amplifier circuit in Rice et al. that was identified by the Examiner (shown in Fig. 10 of the patent) operates to monitor an instantaneous difference between return and feeder currents that are provided to the two input terminals of the operational amplifier (see col. 10, lines 44-53). This operational amplifier circuit entirely lacks a switching element between input and output terminals of the operational amplifier, because the operational amplifier circuit is not intended to provide two different ranges of amplification or gain. Rather, the operational amplifier circuit is intended to provide an indication when there is an imbalance between the return and feeder currents of the generator, and thus provide ground fault detection (see col. 10, lines 57-67).

In contrast, Yamaguchi relates to an improvement of an operational amplifier circuit that inherently includes a switching element between input and output terminals of the operational amplifier. That is, Yamaguchi specifically relates to a type of operational amplifier circuit that operates in two amplification states. This is a totally

different purpose than that of the operational amplifier circuit in Rice et al. Indeed, the Applicants are unable to find any rationale within Yamaguchi as to why one would wish to employ an operational amplifier circuit with a switching element in Rice et al. Similarly, the Applicants are unable to find any suggestion within Rice et al. as to why an operational amplifier circuit such as that disclosed by Yamaguchi would be applicable or of value in performing the operations addressed by Rice et al. such as ground fault detection.

Not only do Rice et al. and Yamaguchi fail to provide a suggestion to combine one another, both references fail to provide a suggestion to combine one another to arrive at the Applicants' claimed invention. In particular, the Applicants are unable to find within Rice et al. any suggestion to use an operational amplifier circuit in conjunction with a switching element in order to switch the amplification of a signal indicative of an alternator current, so that alternator currents at a wide variety of levels can be accurately sensed. Additionally, the Applicants are unable to find any suggestion within Yamaguchi to use an operational amplifier circuit with a switching element between the input and output ports of the operational amplifier in the context of measuring alternator currents, much less to switch the gain of the operational amplifier to allow for sensing alternator currents at a variety of levels. Indeed, the Applicants are unable to find within Yamaguchi any indication that its operational amplifier circuit is intended to provide different levels of amplification for any purpose. Rather, Yamaguchi appears to presume the existence of an operational amplifier circuit with a switching element between the input and output terminals of the operational amplifier, and provides an improvement whereby the ON resistance of that switching element does not

negatively affect the gain of the amplifier (see the Abstract of Yamaguchi).

For all of these reasons, therefore, the Applicants respectfully submit that the pending independent claims 1, 11 and 14 are allowable over Rice et al. in view of Yamaguchi. Further, the Applications respectfully submit that each of pending claims 3-10, 12-13 and 15-21, which respectively depend from claims 1, 11 and 14, also are allowable over the cited prior art references.

FURTHER RESPONSE TO EXAMINER'S COMMENTS IN PARAGRAPH 9 OF THE OFFICE ACTION

In paragraph 9 of the Office Action, the Examiner stated that, with regard to claims 4, 5, 8-9 and 11-13, it should be emphasized that "apparatus claims must be structurally distinguishable from the prior art". The Applicants respectfully submit that, as discussed above, pending independent claims 1, 11 and 14 are structurally distinguishable from the cited references, alone or in combination. In particular, for example, neither Rice et al. nor Yamaguchi appears to disclose a processor that is coupled to the output of an operational amplifier, and further coupled to a switching element that in turn is coupled between the input and output ports of that operational amplifier.

Additionally, the processor (or processing means) as claimed by the Applicants performs specific functions insofar as the processor controls a switching element (or modification means) based upon the level of the alternator current. Because the processor is designed to operate in this way, the processor should be viewed as a special processing structure that is different from that of other processors that do not operate in this way (see, e.g., *In re Alappat*, 33 F.3d 1526, 1545, 31 USPQ 2d 1545 (Fed. Cir. 1994)). Thus, the processor

of the claimed invention has a different structure than the processor disclosed in Rice et al., which does not operate in the same way, and also has a different structure than that disclosed in Yamaguchi, which does not appear to disclose any processor.

For at least these reasons, therefore, the Applicants further submit that the pending independent claims 1, 11 and 14, as well as the dependent claims 2-10, 12-13 and 15-21 are allowable over the cited references.

* * *

Conclusion

In view of the amendments to the claims and the Remarks being submitted herewith, and in view of the distinctions between the presently claimed subject matter and the teachings of the cited references, the Applicants respectfully request reconsideration and allowance of the present application.

The Applicants wish to invite the Examiner to telephone the Applicants' attorney at the number listed below if discussion with the Applicants' attorney would be of assistance to the Examiner or further the prosecution of the present application.

Respectfully submitted,

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VERSION SHOWING CHANGES TO CLAIMS

10. (Amended) The system of claim 1, wherein the operational amplifier includes an additional input, and further comprising:

an additional input resistor coupled to the additional input, and;

[coupled between a voltage source and the additional input,] an additional feedback resistor coupled **between a voltage source and the additional input, wherein the additional feedback resistor is further coupled** in parallel with a combination of an additional adjustment resistor and an additional switching element.

11. (Amended) A system for accurately sensing current levels within an alternator, the system comprising:

an amplification means for amplifying or reducing a first signal indicative of a current level within the alternator to produce a second signal indicative of the current level;

a modification means for adjusting the level of amplification or reduction of the amplification means; and

a processing means for controlling the modification means **based upon at least one of the second signal and a third signal based upon the second signal,** and for processing at least one of the second signal and **[a] the** third signal **[based upon the second signal]** to determine a current measurement value.